Hall Ticket Number:

Code No.: 6215 M

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. I Year (ECE) II-Semester (Make Up) Examinations, August-2016

(Embedded Systems & VLSI Design)

Design for Testability

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 X 2=20 Marks)

1. Justify, the term primitive cube being used for a logic gate.
2. Explain what 'Reconvergent Fan out' is with a suitable example.
3. Bring out the importance of fault modelling.
4. Differentiate between single stuck and multiple stuck fault models.
5. Explain what deterministic test generation for fault detection in a combinational circuit is?
6. Describe the PODEM algorithm for test generation.
7. Write about ad hoc approach for introducing testability into VLSI designs.
8. Highlight the importance of shadow registers.
9. Compare production and field testing.
10. Explain what physical segmentation is?

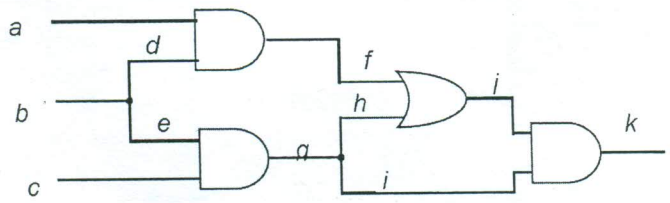
Part-B (5 × 10 = 50 Marks)
(All bits carry equal marks)

11. a) Explain internal representation of a circuit with a suitable example.

    b) Write truth tables for NAND and NOR gates in 5 valued logic. What is the application of five valued logic?

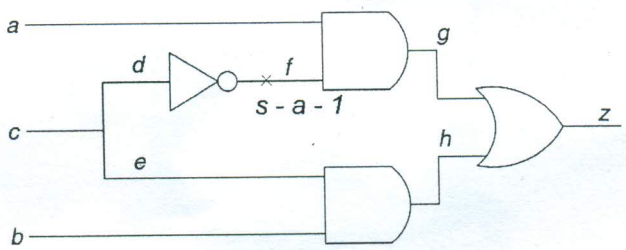
12. a) Differentiate between detectable and undetectable faults with suitable examples.

    b) Identify the fault sites in the following combinational circuit and arrive at a set of collapsed faults after equivalent and dominance collapsing.



13. a) Discuss the 'line justification' and 'error propagation' algorithms for fan out free circuits.

    b) Generate a test using D algorithm for detecting the given fault in the following combinational circuit.



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14. a) Discuss how scan registers can be used to inject and extract test signals in logic circuits.

    b) Draw the chip architecture of IEEE 1149.1 and explain the test procedure.

15. a) Explain the operation of any two test pattern generators.

    b) Describe any two specific BIST architectures.

16. a) Explain what controlling value and inversion value are for a logic gate and discuss the element evaluation based on these parameters.

    b) Differentiate between serial fault simulation and parallel fault simulation.

17. Write short notes on any ***two*** of the following:

    a) Functional testing.

    b) Partitioning large combinational circuits to improve testability.

    c) Adaptive test generation.